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Day : Tuesday
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Inventor Name Search Result

Your Search was:

Last Name = OHLHOFF
First Name = CARSTEN

Application#	Patent#	Status	Date Filed	Title	Inventor Name
09630972	6549028	150	08/02/2000	ARRANGEMENT AND METHOD FOR TESTING A MULTIPLICITY OF SEMICONDUCTOR CHIPS AT THE WAFER LEVEL	OHLHOFF, CARSTEN
09737057	6504394	150	12/14/2000	CONFIGURATION FOR TRIMMING REFERENCE VOLTAGES IN SEMICONDUCTOR CHIPS, IN PARTICULAR SEMICONDUCTOR MEMORIES	OHLHOFF, CARSTEN
09740633	6657452	150	12/18/2000	CONFIGURATION FOR MEASUREMENT OF INTERNAL VOLTAGES OF AN INTEGRATED SEMICONDUCTOR APPARATUS	OHLHOFF, CARSTEN
10035866	6661718	150	12/31/2001	TESTING DEVICE FOR TESTING A MEMORY	OHLHOFF, CARSTEN
10154343	6671221	150	05/23/2002	SEMICONDUCTOR CHIP WITH TRIMMABLE OSCILLATOR	OHLHOFF, CARSTEN
10158031	6639856	150	05/30/2002	MEMORY CHIP HAVING A TEST MODE AND METHOD FOR CHECKING MEMORY CELLS OF A REPAIRED MEMORY CHIP	OHLHOFF, CARSTEN
10200633	Not Issued	90	07/22/2002	DATA GENERATOR FOR GENERATING TEST DATA FOR WORD-ORIENTED SEMICONDUCTOR MEMORIES	OHLHOFF, CARSTEN
10243067	6756787	150	09/13/2002	INTEGRATED CIRCUIT HAVING A CURRENT MEASURING UNIT	OHLHOFF, CARSTEN
10360456	6670665	150	02/06/2003	MEMORY MODULE WITH IMPROVED ELECTRICAL PROPERTIES	OHLHOFF, CARSTEN
10425224	Not Issued	41	04/29/2003	Method and apparatus for masking known fails during memory tests readouts	OHLHOFF, CARSTEN
10452485	Not Issued	93	06/02/2003	TEST DEVICE, TEST SYSTEM AND METHOD FOR TESTING A MEMORY CIRCUIT	OHLHOFF, CARSTEN
10478441	Not Issued	93	05/05/2004	DYNAMIC MEMORY AND METHOD FOR TESTING A DYNAMIC MEMORY	OHLHOFF, CARSTEN

10613367	Not Issued	71	07/03/2003	Test circuit and method for testing an integrated memory circuit	OHLHOFF, CARSTEN
10675761	6891431	150	09/30/2003	INTEGRATED SEMICONDUCTOR CIRCUIT CONFIGURATION	OHLHOFF, CARSTEN
10754455	Not Issued	41	01/09/2004	Memory module, test system and method for testing one or a plurality of memory modules	OHLHOFF, CARSTEN
11270025	Not Issued	25	11/09/2005	Electronic circuit	OHLHOFF, CARSTEN
11356713	Not Issued	19	02/17/2006	Test apparatus and method for testing a circuit unit	OHLHOFF, CARSTEN
11397790	Not Issued	20	04/04/2006	Method and apparatus for masking known fails during memory tests readouts	OHLHOFF, CARSTEN

Inventor Search Completed: No Records to Display.

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Inventor Name Search Result

Your Search was:

Last Name = BEER
First Name = PETER

Application#	Patent#	Status	Date Filed	Title	Inventor Name
09740633	6657452	150	12/18/2000	CONFIGURATION FOR MEASUREMENT OF INTERNAL VOLTAGES OF AN INTEGRATED SEMICONDUCTOR APPARATUS	BEER, PETER
09801963	6612738	150	03/08/2001	METHOD FOR DETERMINING THE TEMPERATURE OF A SEMICONDUCTOR CHIP AND SEMICONDUCTOR CHIP WITH TEMPERATURE MEASURING CONFIGURATION	BEER, PETER
09980601	Not Issued	160	01/01/0001	Integrated sram memory cell	BEER, PETER
10125089	6639861	150	04/18/2002	INTEGRATED MEMORY AND METHOD FOR TESTING AN INTEGRATED MEMORY	BEER, PETER
10131374	6784683	150	04/24/2002	CIRCUIT CONFIGURATION FOR SELECTIVELY TRANSMITTING INFORMATION ITEMS FROM A MEASURING DEVICE TO CHIPS ON A WAFER DURING CHIP FABRICATION	BEER, PETER
10151990	6858447	150	05/21/2002	METHOD FOR TESTING SEMICONDUCTOR CHIPS	BEER, PETER
10154343	6671221	150	05/23/2002	SEMICONDUCTOR CHIP WITH TRIMMABLE OSCILLATOR	BEER, PETER
10156536	6737695	150	05/28/2002	MEMORY MODULE HAVING A MEMORY CELL AND METHOD FOR FABRICATING THE MEMORY MODULE	BEER, PETER
10158031	6639856	150	05/30/2002	MEMORY CHIP HAVING A TEST MODE AND METHOD FOR CHECKING MEMORY CELLS OF A REPAIRED MEMORY CHIP	BEER, PETER
10159858	6636447	150	05/31/2002	MEMORY MODULE, METHOD FOR ACTIVATING A MEMORY CELL, AND METHOD FOR REPAIRING A DEFECTIVE MEMORY CELL	BEER, PETER

10178646	Not Issued	161	06/24/2002	Integrated memory circuit and method for reading a data item from a memory cell	BEER, PETER
10190814	6754110	150	07/08/2002	EVALUATION CIRCUIT FOR A DRAM	BEER, PETER
10195194	6740917	150	07/15/2002	INTEGRATED SEMICONDUCTOR MEMORY AND FABRICATION METHOD	BEER, PETER
10202690	6728147	150	07/24/2002	METHOD FOR ON-CHIP TESTING OF MEMORY CELLS OF AN INTEGRATED MEMORY CIRCUIT	BEER, PETER
10243067	6756787	150	09/13/2002	INTEGRATED CIRCUIT HAVING A CURRENT MEASURING UNIT	BEER, PETER
10289913	6829185	150	11/07/2002	METHOD FOR PRECHARGING MEMORY CELLS OF A DYNAMIC SEMICONDUCTOR MEMORY DURING POWER-UP AND SEMICONDUCTOR MEMORY	BEER, PETER
10360456	6670665	150	02/06/2003	MEMORY MODULE WITH IMPROVED ELECTRICAL PROPERTIES	BEER, PETER
10425224	Not Issued	41	04/29/2003	Method and apparatus for masking known fails during memory tests readouts	BEER, PETER
10452485	Not Issued	93	06/02/2003	TEST DEVICE, TEST SYSTEM AND METHOD FOR TESTING A MEMORY CIRCUIT	BEER, PETER
10609874	Not Issued	161	06/30/2003	Memory, module with crossed bit lines, and method for reading the memory module	BEER, PETER
10610186	Not Issued	41	06/30/2003	Memory chip with test logic taking into consideration the address of a redundant word line and method for testing a memory chip	BEER, PETER
10613367	Not Issued	71	07/03/2003	Test circuit and method for testing an integrated memory circuit	BEER, PETER
10627841	6813200	150	07/25/2003	CIRCUIT CONFIGURATION FOR READING OUT A PROGRAMMABLE LINK	BEER, PETER
10653652	6922365	150	09/02/2003	READ-OUT CIRCUIT FOR A DYNAMIC MEMORY CIRCUIT MEMORY CELL ARRAY AND METHOD FOR AMPLIFYING AND READING DATA STORED IN A MEMORY CELL ARRAY	BEER, PETER
10667254	Not Issued	41	09/19/2003	Self-test circuit and a method for testing a memory with the self-test circuit	BEER, PETER
10667256	Not Issued	30	09/19/2003	Test circuit of an integrated memory circuit for coding assessment data and method for testing the memory circuit	BEER, PETER

10675054	6831320	150	09/30/2003	MEMORY CELL CONFIGURATION FOR A DRAM MEMORY WITH A CONTACT BIT TERMINAL FOR TWO TRENCH CAPACITORS OF DIFFERENT ROWS	BEER, PETER
10675761	6891431	150	09/30/2003	INTEGRATED SEMICONDUCTOR CIRCUIT CONFIGURATION	BEER, PETER
10676588	Not Issued	41	10/01/2003	Test system and method for testing memory circuits	BEER, PETER
10676596	Not Issued	93	10/01/2003	MEMORY CIRCUIT AND METHOD FOR READING OUT DATA	BEER, PETER
10676597	Not Issued	61	10/01/2003	Memory circuit with a test mode for writing test data	BEER, PETER
10704205	Not Issued	41	11/06/2003	Method for writing to a defect address memory, and test circuit having a defect address memory	BEER, PETER
10723289	7009869	150	11/25/2003	DYNAMIC MEMORY CELL	BEER, PETER
10754455	Not Issued	41	01/09/2004	Memory module, test system and method for testing one or a plurality of memory modules	BEER, PETER
10798245	6862234	150	03/11/2004	METHOD AND TEST CIRCUIT FOR TESTING A DYNAMIC MEMORY CIRCUIT	BEER, PETER
10831466	6985390	150	04/23/2004	INTEGRATED MEMORY CIRCUIT HAVING A REDUNDANCY CIRCUIT AND A METHOD FOR REPLACING A MEMORY AREA	BEER, PETER
10888649	7038956	150	07/09/2004	APPARATUS AND METHOD FOR READING OUT DEFECT INFORMATION ITEMS FROM AN INTEGRATED CHIP	BEER, PETER
10920210	Not Issued	30	08/18/2004	Integrated memory having a test circuit for functional testing of the memory	BEER, PETER
10923639	Not Issued	93	08/20/2004	MRAM WITH VERTICAL STORAGE ELEMENT IN TWO LAYER-ARRANGEMENT AND FIELD SENSOR	BEER, PETER
10933645	Not Issued	30	09/03/2004	Method and apparatus for checking output signals of an integrated circuit	BEER, PETER
11117713	Not Issued	30	04/29/2005	Adiabatic rotational switching memory element including a ferromagnetic decoupling layer	BEER, PETER
11271927	Not Issued	20	11/14/2005	System and method for monitoring the status and progress of a technical process or of a technical project	BEER, PETER
11397790	Not Issued	20	04/04/2006	Method and apparatus for masking known fails during memory tests readouts	BEER, PETER

08257538	Not Issued	161	06/09/1994	APPARATUS FOR MEASURING DEFLECTION OF AXLES	BEER, PETER DE
09446262	6398303	150	05/05/2000	SEAT	BEERBAUM, PETER
10354272	6785875	150	01/28/2003	METHODS AND APPARATUS FOR FACILITATING PHYSICAL SYNTHESIS OF AN INTEGRATED CIRCUIT DESIGN	BEEREL, PETER
10620330	6854096	150	07/14/2003	OPTIMIZATION OF CELL SUBTYPES IN A HIERARCHICAL DESIGN FLOW	BEEREL, PETER
10977362	Not Issued	160	10/28/2004	Optimization of cell subtypes in a hierarchical design flow	BEEREL, PETER
11271323	Not Issued	20	11/10/2005	Logic synthesis of multi-level domino asynchronous pipelines	BEEREL, PETER
60404359	Not Issued	159	08/15/2002	P2N sizing tool - path based sizing	BEEREL, PETER

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